

**Family list**

7 family members for:

**WO0175853**

Derived from 4 applications.

- 1 Driver circuit for organic electroluminescent device**  
Publication info: **GB0007879D D0** - 2000-05-17  
**GB2360870 A** - 2001-10-03
- 2 Pixel driver for an organic electroluminescent device**  
Publication info: **GB0016815D D0** - 2000-08-30  
**GB2364592 A** - 2002-01-30
- 3 Pixel driver for an organic electroluminescent device**  
Publication info: **GB0016816D D0** - 2000-08-30  
**GB2364593 A** - 2002-01-30
- 4 ORGANIC ELECTROLUMINESCENT DEVICE COMPENSATED PIXEL DRIVER CIRCUIT**  
Publication info: **WO0175853 A1** - 2001-10-11

---

Data supplied from the **esp@cenet** database - Worldwide

## (12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
11 October 2001 (11.10.2001)

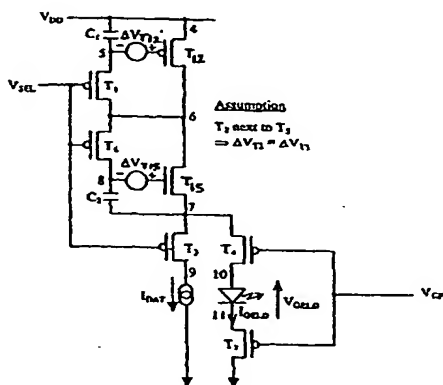
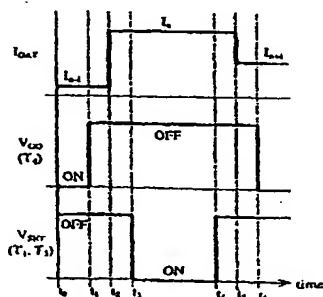
PCT

(10) International Publication Number  
**WO 01/75853 A1**(51) International Patent Classification<sup>7</sup>: **G09G 3/32**

[GB/GB]; Epson Cambridge Laboratory, 8c King's Parade, Cambridge CB2 1SJ (GB).

(21) International Application Number: **PCT/GB01/01460**(22) International Filing Date: **30 March 2001 (30.03.2001)**(74) Agent: **STURT, Clifford, Mark**; Miller Sturt Kenyon, 9 John Street, London WC1N 2ES (GB).(25) Filing Language: **English**(81) Designated States (*national*): **JP, US.**(26) Publication Language: **English**(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).(30) Priority Data:  
**0007879.0 31 March 2000 (31.03.2000) GB**(71) Applicant (*for all designated States except US*): **SEIKO EPSON CORPORATION [JP/JP]; 4-1, Nishishinjuku 2-chome, Shinjuku-ku, Tokyo 163-0811 (JP).****Published:**  
— *with international search report*

(72) Inventor; and

(75) Inventor/Applicant (*for US only*): **TAM, Simon***For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*(54) Title: **ORGANIC ELECTROLUMINESCENT DEVICE COMPENSATED PIXEL DRIVER CIRCUIT**(57) Abstract: A compensated pixel driver circuit comprises a p-channel transistor and an n-channel transistor connected as a complementary pair of transistors to provide analog control of the drive current for an organic electroluminescent device (OLED). The transistors, being of opposite channel, compensate for any variation in threshold voltage  $\Delta V_T$  and therefore provide a drive current to the OLED which is relatively independent of  $\Delta V_T$ . The complementary pair of transistors can be applied to either voltage driving or current driving pixel driver circuits.

WO 01/75853 A1

## Organic ElectroLuminescent Device Compensated Pixel Driver Circuit

The present invention relates to an organic electroluminescent device and particularly to a compensated pixel driver circuit thereof.

An organic electroluminescent device (OELD) consists of a light emitting polymer (LEP) layer sandwiched between an anode layer and a cathode layer. Electrically, this device operates like a diode. Optically, it emits light when forward biased and the intensity of the emission increases with the forward bias current. It is possible to construct a display panel with a matrix of OELDs fabricated on a transparent substrate and with one of the electrode layers being transparent. It is also possible to integrate the driving circuit on the same panel by using low temperature polysilicon thin film transistor (TFT) technology.

In a basic analog driving scheme for an active matrix OELD display, a minimum of two transistors are required per pixel. Such a driving scheme is illustrated in Figure 1. Transistor  $T_1$  is provided to address the pixel and transistor  $T_2$  is provided to convert a data voltage signal  $V_{Data}$  into current which drives the OELD at a designated brightness. The data signal is stored by a storage capacitor  $C_{storage}$  when the pixel is not addressed. Although p-channel TFTs are shown in the figure, the same principle can also be applied for a circuit utilising n-channel TFTs.

There are problems associated with TFT analog circuits and OELDs do not act like perfect diodes. The LEP material does, however, have relatively uniform characteristics. Due to the nature of the TFT fabrication technique, spatial variation of the TFT characteristics exists over the extent of the display panel. One of the most important considerations in a TFT analog circuit is the variation of threshold voltage,  $\Delta V_T$ , from

device to device. The effect of such variation in an OLED display, exacerbated by the non perfect diode behaviour, is the non-uniform pixel brightness over the display area of the panel, which seriously affects the image quality. Therefore, a built-in compensation circuit is required.

A simple threshold voltage variation compensation, current driven, circuit has been proposed. The current driven circuit, also known as the current programmed threshold voltage compensation circuit, is illustrated in figure 2. In this circuit, transistor  $T_1$  is provided for addressing the pixel. Transistor  $T_2$  operates as an analog current control to provide the driving current to the OLED. Transistor  $T_3$  connects between the drain and gate of transistor  $T_2$  and toggles transistor  $T_2$  to act either as a diode or in a saturation mode. Transistor  $T_4$  acts as a switch in response to an applied waveform  $V_{GP}$ . Either Transistor  $T_1$  or transistor  $T_4$  can be ON at any one time. Initially, at time  $t_0$  shown in the timing diagram of Figure 2, transistors  $T_1$  and  $T_3$  are OFF, and transistor  $T_4$  is ON. When transistor  $T_4$  is OFF, transistors  $T_1$  and  $T_3$  are ON, and a current  $I_{DAT}$  of known value is allowed to flow into the OLED, through transistor  $T_2$ . This is the programming stage because the threshold voltage of transistor  $T_2$  is measured with transistor  $T_3$  turned ON, which shorts the drain and gate of transistor  $T_2$ . Hence transistor  $T_2$  operates as a diode while the programming current is allowed to flow through transistors  $T_1$  and  $T_2$  and into the OLED. The detected threshold voltage of transistor  $T_2$  is stored by a capacitor  $C_1$  connected between the gate and source terminals of transistor  $T_2$  when transistors  $T_3$  and  $T_1$  are switched OFF. Transistor  $T_4$  is then turned ON by driving waveform  $V_{GP}$  and the current through the OLED is now provided by supply  $V_{DD}$ . If the slope of the output

characteristics for transistor  $T_2$  were flat, the reproduced current would be the same as the programmed current for any threshold voltage of  $T_2$  detected and stored in capacitor  $C_1$ . However, by turning ON transistor  $T_4$ , the drain-source voltage of transistor  $T_2$  is pulled up, so a flat output characteristic will maintain the reproduced current at the same level as the programmed current. Note that  $\Delta V_{T2}$  shown in figure 2 is imaginary, not real. It has been used solely to represent the threshold voltage of transistor  $T_2$ .

A constant current is provided, in theory, during a subsequent active programming stage, which is signified by the time interval  $t_2$  to  $t_3$  in the timing diagram shown in figure 2. The reproduction stage starts at time  $t_6$ .

The circuit of Figure 2 does provide an improvement over the circuit shown in Figure 1 but variations in the threshold value of the control transistor are not fully compensated and variations in image brightness over the display area of the panel remain.

The present invention seeks to provide, therefore, an improved compensated pixel driver circuit in which variations in the threshold voltages of the pixel driver transistor can be further compensated, thereby providing a more uniform pixel brightness over the display area of the panel and, therefore, improved image quality.

According to a first aspect of the present invention there is provided a compensated pixel driver circuit for an electroluminescent device, the circuit comprising an n-channel transistor and a complementary p-channel transistor connected so as to operatively control, in combination, the current supplied to the electroluminescent device.

Preferably, the compensated pixel driver circuit also comprises respective storage capacitors for the n-channel and p-channel transistors and respective switching means

connected so as to establish when operative respective paths to the n-channel and p-channel transistors for respective data voltage pulses.

Advantageously, the compensated pixel driver circuit may also comprise respective storage capacitors for storing a respective operating voltage of the n-channel and the p-channel transistors during a programming stage, a first switching means connected so as to establish when operative a first current path from a source of current data signals through the n-channel and p-channel transistors and the electroluminescent device during the programming stage, and a second switching means connected to establish when operative a second current path through the n-channel and p-channel transistors and the electroluminescent device during a reproduction stage.

In a further embodiment, the first switching means and the source of current data signals are connected so as to provide when operative a current source for the electroluminescent device.

In an alternative embodiment, the first switching means the source of current data signals are connected so as to provide when operative a current sink for the electroluminescent device.

According to a second aspect of the present invention there is also provided a method of compensating the supply current to an electroluminescent device comprising providing an n-channel transistor and a p-channel transistor connected so as to operatively control, in combination, the supply current to the electroluminescent device.

Preferably, the method further comprises providing respective storage capacitors for the n-channel and p-channel transistors and respective switching means connected so as to establish when operative respective paths to the n-channel and p-channel transistors for

respective data voltage pulses thereby to establish, when operative, a voltage driver circuit for the electroluminescent device.

Advantageously, the method may comprise providing a programming stage during which the n-channel and p-channel transistors are operated in a first mode and wherein a current path from a source of current data signals is established through the n-channel and the p-channel transistors and the electroluminescent device and wherein a respective operating voltage of the n-channel transistor and the p-channel transistor is stored in respective storage capacitors, and a reproduction stage wherein a second mode and a second current path is established through the n-channel transistor and the p-channel transistor and the electroluminescent device.

According to a third aspect of the present invention, there is also provided an organic electroluminescent display device comprising a compensated pixel driver circuit as claimed in any one of claims 1 to 11.

The present invention will now be described by way of further example only, with reference to the accompanying drawings in which:-

Fig. 1 shows a conventional OLED pixel driver circuit using two transistors;

Fig. 2 shows a known current programmed OLED driver circuit with threshold voltage compensation;

Fig. 3 illustrates the concept of a compensated pixel driver circuit including a complementary pair of driver transistors for providing threshold voltage compensation in accordance with the present invention;

Fig. 4 shows plots of characteristics for the complementary driver transistors illustrated in Fig. 3 for various levels of threshold voltages;

Fig. 5 shows a compensated pixel driver circuit arranged to operate as a voltage driver circuit in accordance with a first embodiment of the present invention.

Fig. 6 shows a compensated pixel driver circuit arranged to operate as a current programmed driver circuit in accordance with a second embodiment of the present invention;

Fig. 7 shows a compensated current programmed driver circuit in accordance with a third embodiment of the present invention, and

Figs 8 to 11 show SPICE simulation results for the circuit illustrated in Fig. 6.

The concept of a compensated pixel driver circuit according to the present invention is illustrated in Fig. 3. An OELD device is coupled between two transistors  $T_{11}$  and  $T_{12}$  which operate, in combination, as an analog current control for the current flowing through the OELD. Transistor  $T_{11}$  is a p-channel transistor and transistor  $T_{12}$  is an n-channel transistor which act therefore, in combination, as a complementary pair for analog control of the current through the OELD.

As mentioned previously, one of the most important parameters in a TFT analog circuit design is the threshold voltage  $V_T$ . Any variation,  $\Delta V_T$  within a circuit has a significant effect on the overall circuit performance. Variations in the threshold voltage can be viewed as a rigid horizontal shift of the source to drain current versus the gate to source voltage characteristic for the transistor concerned and are caused by the interface charge at the gate of the transistor.

It has been realised with the present invention that in an array of TFT devices, in view of the fabrication techniques employed, neighbouring or relatively close TFT's have a high probability of exhibiting the same or an almost similar value of threshold voltage  $\Delta V_T$ . Furthermore, it has been realised that as the effects of the same  $\Delta V_T$  on p-channel and n-



channel TFT's are complementary, compensation for variations in threshold voltage  $\Delta V_T$  can be achieved by employing a pair of TFT's, one p-channel TFT and one n-channel TFT, to provide analog control of the driving current flowing to the OELD. The driving current can, therefore, be provided independently of any variation of the threshold voltage. Such a concept is illustrated in figure 3.

Figure 4 illustrates the variation in drain current, that is the current flowing through the OELD shown in figure 3, for various levels of threshold voltage  $\Delta V_T$ ,  $\Delta V_{T1}$ ,  $\Delta V_{T2}$  for the transistors  $T_{11}$  and  $T_{12}$ . Voltages  $V_1$ ,  $V_2$  and  $V_D$  are respectively the voltages appearing across transistor  $T_{11}$ ,  $T_{12}$  and the OELD from a voltage source  $V_{DD}$ . Assuming that the transistors  $T_{11}$  and  $T_{12}$  have the same threshold voltage and assuming that  $\Delta V_T = 0$ , then the current flowing through the OELD is given by cross-over point A for the characteristics for the p-channel transistor  $T_{11}$  and the n-channel transistor  $T_{12}$  shown in figure 4. This is shown by value  $I_0$ .

Assuming now that the threshold voltage of the p-channel and n-channel transistors changes to  $\Delta V_{T1}$ , the OELD current  $I_1$  is then determined by crossover point B. Likewise, for a variation in threshold voltage to  $\Delta V_2$ , the OELD current  $I_2$  is given by crossover point C. It can be seen from figure 4 that even with the variations in the threshold voltage there is minimal variation in the current flowing through the OELD.

Figure 5 shows a compensated pixel driver circuit configured as a voltage driver circuit. The circuit comprises p-channel transistor  $T_{12}$  and n-channel transistor  $T_{15}$  acting as a complementary pair to provide, in combination, an analog current control for the OELD. The circuit includes respective storage capacitors  $C_{12}$  and  $C_{15}$  and respective switching transistors  $T_A$  and  $T_B$  coupled to the gates of transistors  $T_{12}$  and  $T_{15}$ . When transistors  $T_A$  and

$T_B$  are switched ON data voltage signals  $V_1$  and  $V_2$  are stored respectively in storage capacitors  $C_{12}$  and  $C_{15}$  when the pixel is not addressed. The transistors  $T_A$  and  $T_B$  function as pass gates under the selective control of addressing signals  $\phi_1$  and  $\phi_2$  applied to the gates of transistors  $T_A$  and  $T_B$ .

Figure 6 shows a compensated driver circuit according to the present invention configured as a current programmed OELD driver circuit. As with the voltage driver circuit, p-channel transistor  $T_{12}$  and n-channel transistor  $T_{15}$  are coupled so as to function as an analog current control for the OELD. Respective storage capacitors  $C_1$ ,  $C_2$  and respective switching transistors  $T_1$  and  $T_6$  are provided for transistors  $T_{12}$  and  $T_{15}$ . The driving waveforms for the circuit are also shown in figure 6. Either transistors  $T_1$ ,  $T_3$  and  $T_6$ , or transistor  $T_4$  can be ON at any one time. Transistors  $T_1$  and  $T_6$  connect respectively between the drain and gate of transistors  $T_{12}$  and  $T_{15}$  and switch in response to applied waveform  $V_{SEL}$  to toggle transistors  $T_{12}$  and  $T_{15}$  to act either as diodes or as transistors in saturation mode. Transistor  $T_3$  is also connected to receive waveform  $V_{SEL}$ . Transistors  $T_1$  and  $T_6$  are both p-channel transistors to ensure that the signals fed through these transistors are at the same magnitude. This is to ensure that any spike currents through the OELD during transitions of the waveform  $V_{SEL}$  are kept to a minimum.

The circuit shown in figure 6 operates in a similar manner to known current programmed pixel driver circuits in that a programming stage and a display stage are provided in each display period but with the added benefit that the drive current to the OELD is controlled by the complementary opposite channel transistors  $T_{12}$  and  $T_{15}$ . Referring to the driving waveforms shown in figure 6, a display period for the driver circuit extends from time  $t_0$  to time  $t_6$ . Initially, transistor  $T_4$  is ON and transistors  $T_1$ ,  $T_3$  and  $T_6$  are OFF. Transistor  $T_4$  is turned OFF at time  $t_1$  by the waveform  $V_{GP}$  and transistors  $T_1$ ,  $T_3$

and  $T_6$  are turned ON at time  $t_3$  by the waveform  $V_{SEL}$ . With transistors  $T_1$  and  $T_6$  turned ON, the p-channel transistor  $T_{12}$  and the complementary n-channel transistor  $T_{15}$  act in a first mode as diodes. The driving waveform for the frame period concerned is available from the current source  $I_{DAT}$  at time  $t_2$  and this is passed by the transistor  $T_3$  when it switches on at time  $t_3$ . The detected threshold voltages of transistors  $T_{12}$  and  $T_{15}$  are stored in capacitors  $C_1$  and  $C_2$ . These are shown as imaginary voltage sources  $\Delta V_{T12}$  and  $\Delta V_{T15}$  in figure 6.

Transistors  $T_1$ ,  $T_3$  and  $T_6$  are then switched OFF at time  $t_4$  and transistor  $T_4$  is switched ON at time  $t_5$  and the current through the OELD is then provided from the source VDD under the control of the p-channel and n-channel transistors  $T_{12}$  and  $T_{15}$  operating in a second mode, i.e. as transistors in saturation mode. It will be appreciated that as the current through the OELD is controlled by the complementary p-channel and n-channel transistors  $T_{12}$  and  $T_{15}$ , any variation in threshold voltage in one of the transistors will be compensated by the other opposite channel transistor, as described previously with respect to figure 4.

In the current programmed driver circuit shown in figure 6, the switching transistor  $T_3$  is coupled to the p-channel transistor  $T_{12}$ , with the source of the driving waveform  $I_{DAT}$  operating as a current source. However, the switching transistor  $T_3$  may as an alternative be coupled to the n-channel transistor  $T_{15}$  as shown in figure 7, whereby  $I_{DAT}$  operates as a current sink. In all other respects the operation of the circuit shown in figure 7 is the same as for the circuit shown in figure 6.

Figures 8 to 11 show a SPICE simulation of an improved compensated pixel driver circuit according to the present invention.

Referring to figure 8, this shows the driving waveforms  $I_{DAT}$ ,  $V_{GP}$ ,  $V_{SEL}$  and three values of threshold voltage, namely -1volt, 0volts and +1volt used for the purposes of simulation to show the compensating effect provided by the combination of the p-channel and n-channel transistors for controlling the current through the OELD. From figure 8, it can be seen that, initially the threshold voltage  $\Delta V_T$  was set at -1volt, increasing to 0volts at  $0.3 \times 10^{-4}$  seconds and increasing again to +1volt at  $0.6 \times 10^{-4}$  seconds. However, it can be seen from figure 9 that even with such variations in the threshold voltage the driving current through the OELD remains relatively unchanged.

The relative stability in the driving current through the OELD can be more clearly seen in figure 10, which shows a magnified version of the response plots shown in figure 9.

It can be seen from figure 10 that, using a value of 0 volts as a base for the threshold voltage  $\Delta V_T$ , that if the threshold voltage  $\Delta V_T$  changes to -1volts there is a change of approximately 1.2% in the drive current through the OELD and if the threshold voltage  $\Delta V_T$  is changed to +1volt, there is a reduction in drive current of approximately 1.7% compared to the drive current when the threshold voltage  $\Delta V_T$  is 0 volts. The variation of drive current of 8.7% is shown for reference purposes only as such a variation can be compensated by gamma correction, which is well known in this art and will not therefore be described in relation to the present invention.

Figure 11 shows that for levels of  $I_{DAT}$  ranging from  $0.2\mu A$  to  $1.0\mu A$ , the improved control of the OELD drive current is maintained by the use of the p-channel and opposite n-channel transistors in accordance with the present invention.

It will be appreciated from the above description that the use of a p-channel transistor and an opposite n-channel transistor to provide, in combination, analog control of

the drive current through an electroluminescent device provides improved compensation for the effects which would otherwise occur with variations in the threshold voltage of a single p-channel or n-channel transistor.

Preferably, the TFT n-channel and p-channel transistors are fabricated as neighbouring or adjacent transistors during the fabrication of an OLED display so as to maximise the probability of the complementary p-channel and n-channel transistors having the same value of threshold voltage  $\Delta V_T$ . The p-channel and n-channel transistors may be further matched by comparison of their output characteristics.

The improved compensated pixel driver circuit of the present invention may be used in display devices incorporated in many types of equipment such as mobile displays e.g. mobile phones, laptop personal computers, DVD players, cameras, field equipment; portable displays such as desktop computers, CCTV or photo albums; or industrial displays such as control room equipment displays.

The foregoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

**CLAIMS**

1. A compensated pixel driver circuit for an electroluminescent device, the circuit comprising an n-channel transistor and a complementary p-channel transistor connected so as to operatively control, in combination, the current supplied to the electroluminescent device.
2. A compensated pixel driver circuit as claimed in claim 1, wherein the complementary n-channel and p-channel transistors comprise polysilicon thin film transistors.
3. A compensated pixel driver circuit as claimed in claim 2, wherein the complementary n-channel and p-channel transistors are spatially arranged in close proximity to each other for providing a complementary pair of n-channel and p-channel transistors having approximately equal threshold voltages.
4. A compensated pixel driver circuit as claimed in any one of claims 1 to 3 connected so as to establish when operative a voltage driver circuit comprising respective storage capacitors for the n-channel and p-channel transistors and respective switching means connected so as to establish when operative respective paths to the n-channel and p-channel transistors for respective data voltage pulses.

5. A compensated pixel driver circuit as claimed in any one of claims 1 to 3 comprising respective storage capacitors for storing a respective operating voltage of the n-channel and the p-channel transistors during a programming stage, a first switching means connected so as to establish when operative a first current path from a source of current data signals through the n-channel and p-channel transistors and the electroluminescent device during the programming stage, and a second switching means connected to establish when operative a second current path through the n-channel and p-channel transistors and the electroluminescent device during a reproduction stage.

6. A compensated pixel driver circuit as claimed in claim 5, wherein the first switching means and the source of current data signals are connected so as to provide when operative a current source for the electroluminescent device.

7. A compensated pixel driver circuit as claimed in claim 5, wherein the first switching means and the source of current data signals are connected so as to provide when operative a current sink for the electroluminescent device.

8. A compensated pixel driver circuit as claimed in any one of claims 5 to 7, further comprising respective further switching means respectively connected to bias the n-channel transistor and the p-channel transistor to act as diodes during the programming stage.

9. A compensated pixel driver circuit as claimed in claim 8, wherein the respective further switching means comprise p-channel transistors.

10. A compensated pixel driver circuit as claimed in any one of claims 5 to 9, wherein the circuit is implemented with polysilicon thin film transistors.
11. A compensated pixel driver circuit as claimed in claim 4, wherein the circuit is implemented using polysilicon thin film transistors.
12. A method of compensating the supply current to an electroluminescent device comprising providing an n-channel transistor and a p-channel transistor connected so as to operatively control, in combination, the supply current to the electroluminescent device.
13. A method as claimed in claim 11, comprising the further step of providing the n-channel transistor and the p-channel transistor as polysilicon thin film transistors.
14. A method as claimed in claim 12 comprising the further step of spatially arranging the n-channel and p-channel polysilicon thin film transistors in close proximity to each other.
15. A method as claimed in any one of claims 12 to 14 comprising providing respective storage capacitors for the n-channel and p-channel transistors and respective switching means connected so as to establish when operative respective paths to the n-channel and p-channel transistors for respective data voltage pulses thereby to establish, when operative, a voltage driver circuit for the electroluminescent device.



16. A method as claimed in any one of claims 12 to 14 comprising providing a programming stage during which the n-channel and p-channel transistors are operated in a first mode and wherein a current path from a source of current data signals is established through the n-channel and the p-channel transistors and the electroluminescent device and wherein a respective operating voltage of the n-channel transistor and the p-channel transistor is stored in respective storage capacitors, and a reproduction stage wherein a second mode and a second current path is established through the n-channel transistor and the p-channel transistor and the electroluminescent device.

17. A method as claimed in claim 15, wherein the first mode comprises operating the n-channel and p-channel transistors as diodes.

18. An organic electroluminescent display device comprising a compensated pixel driver circuit as claimed in any one of claims 1 to 11.

1/7

Fig.1.

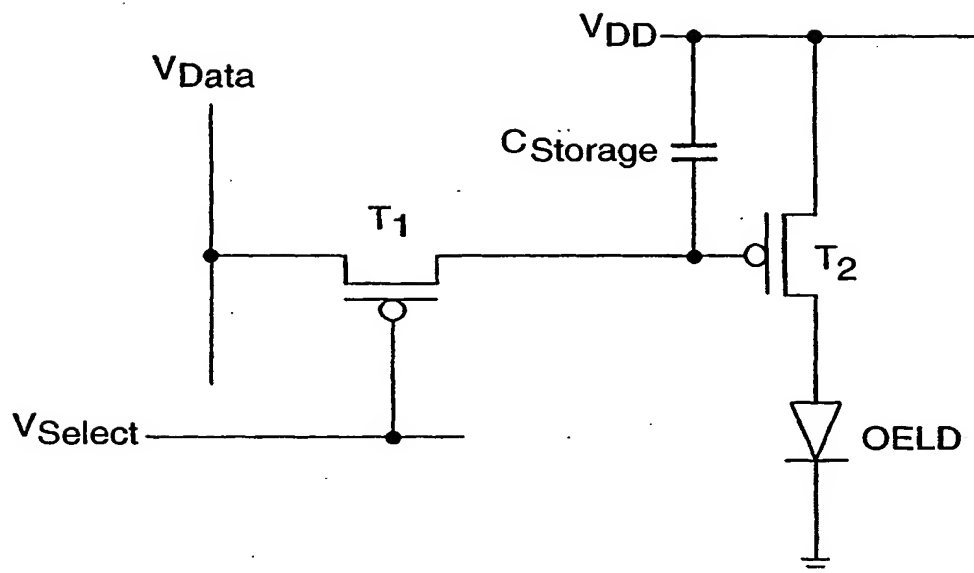


Fig.2.

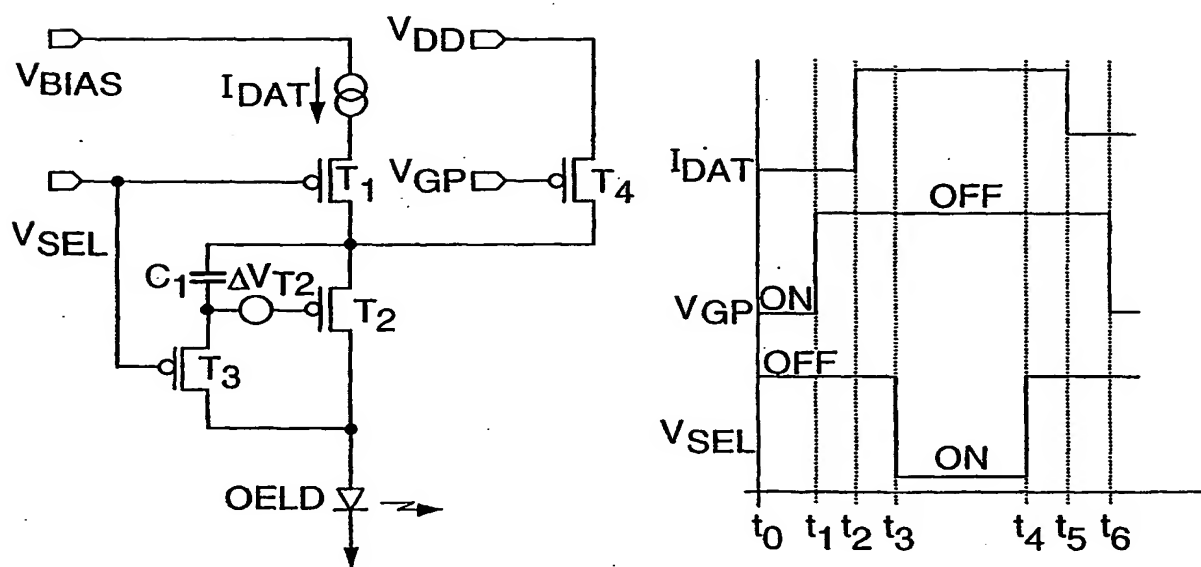


Fig.3.

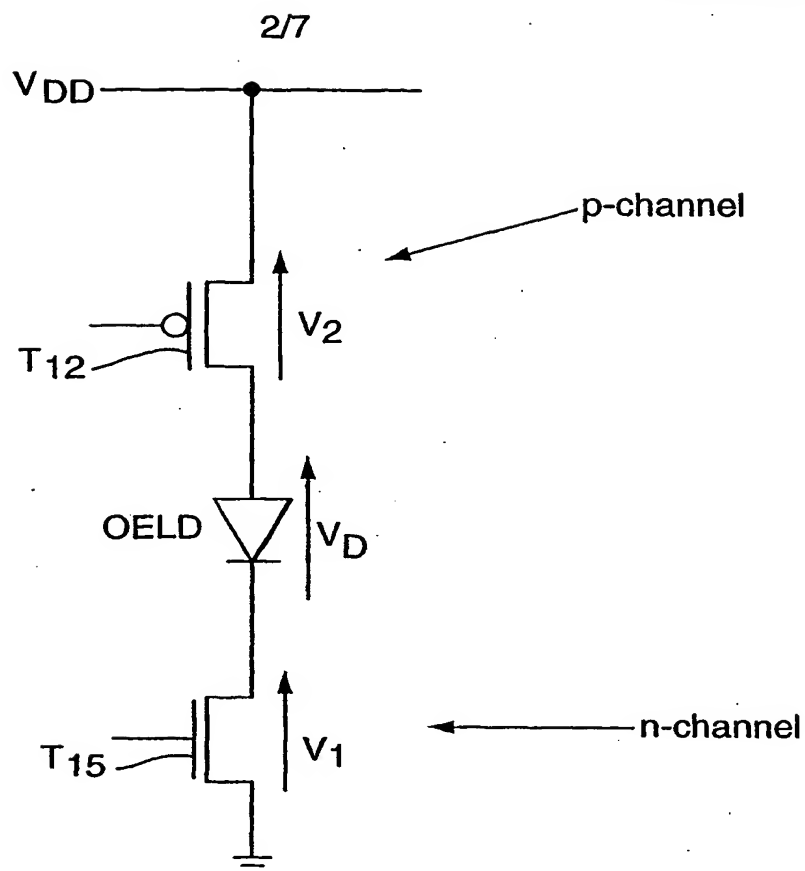


Fig.4.

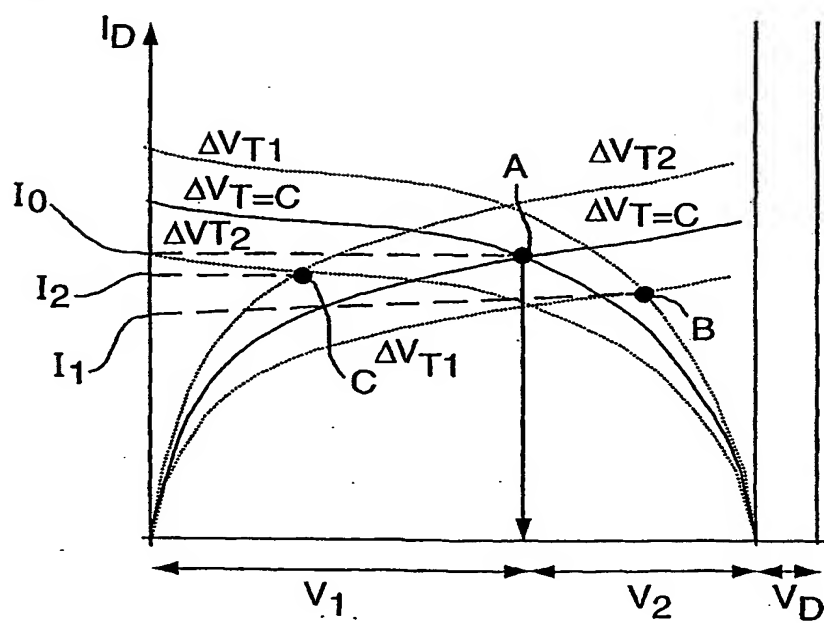


Fig.5.

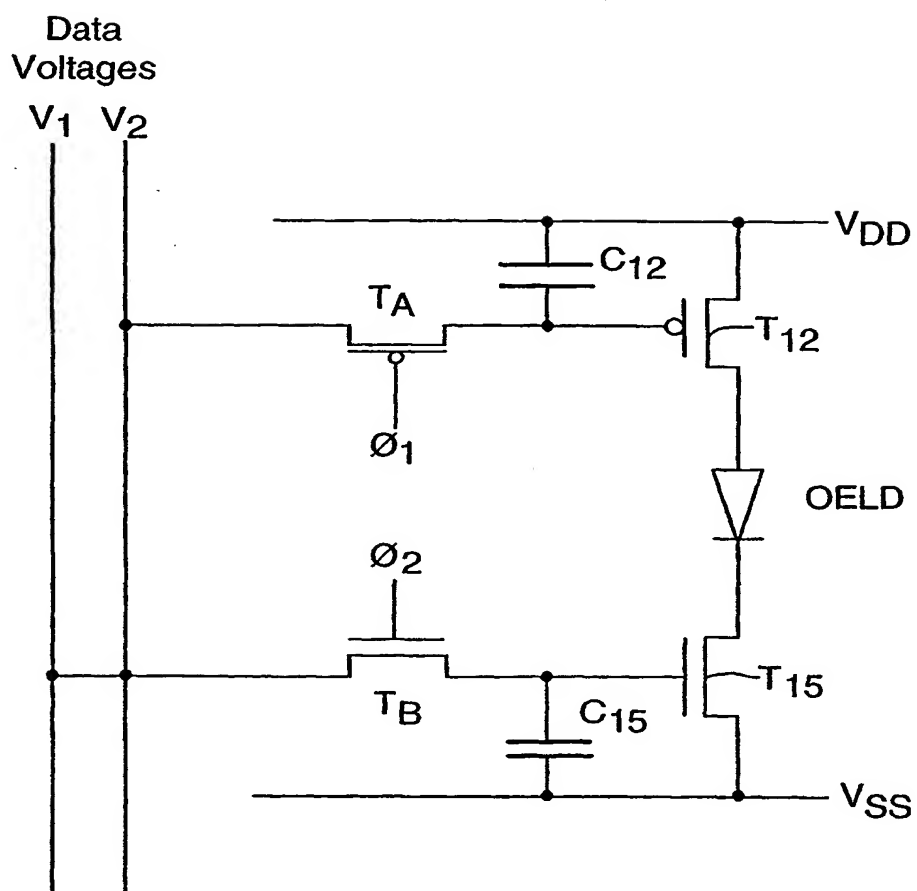
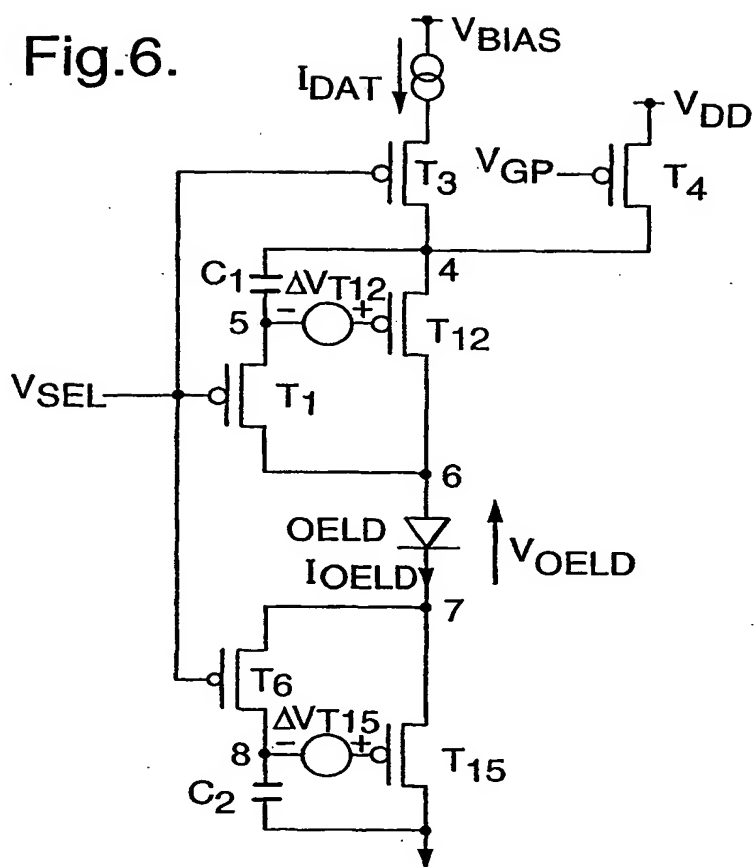
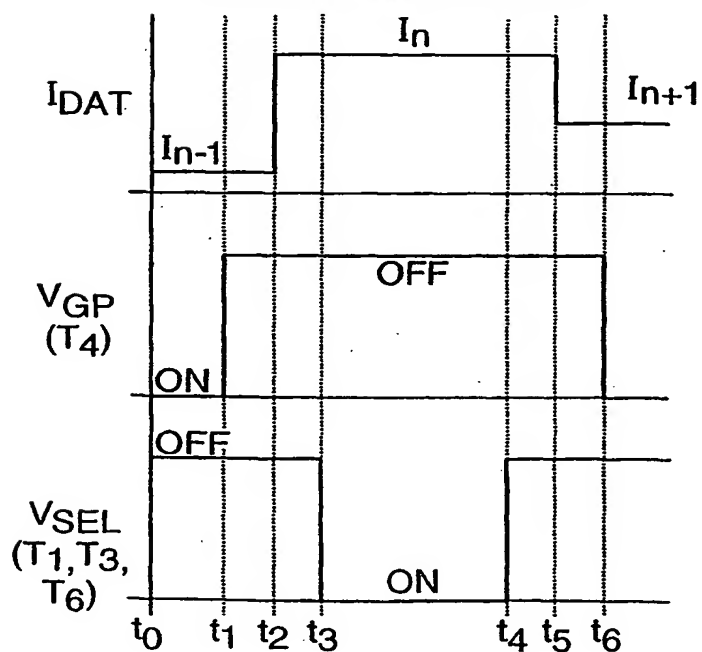


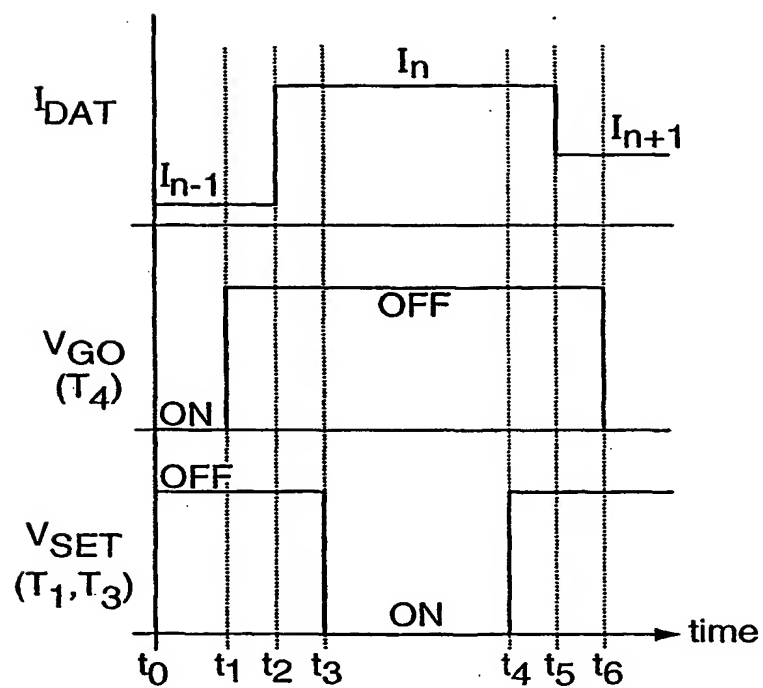
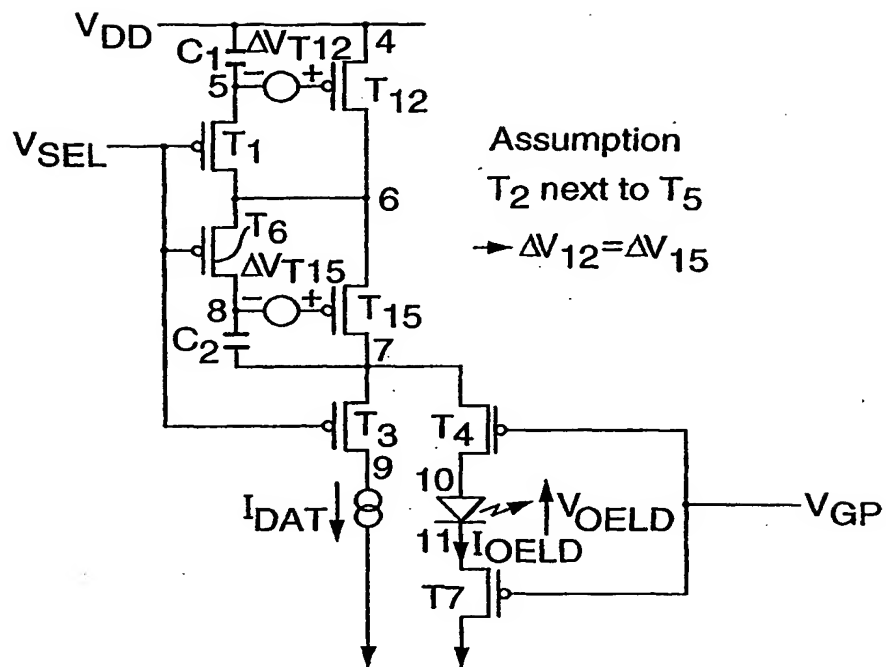
Fig.6.



## DRIVING WAVEFORM



**Fig.7.**



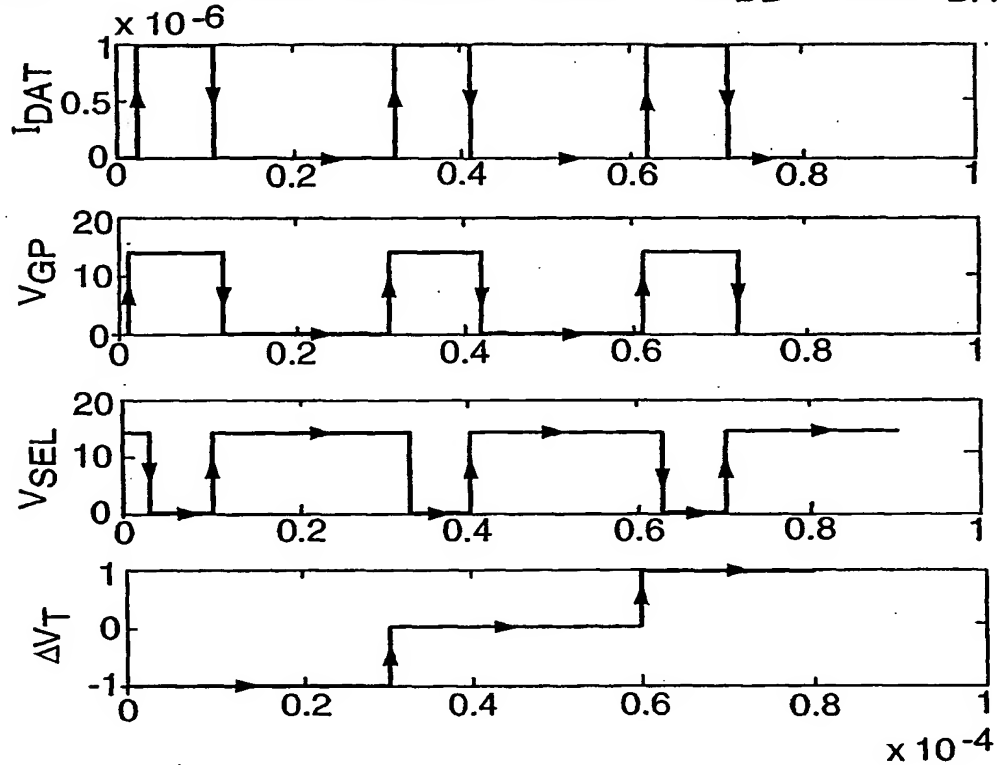
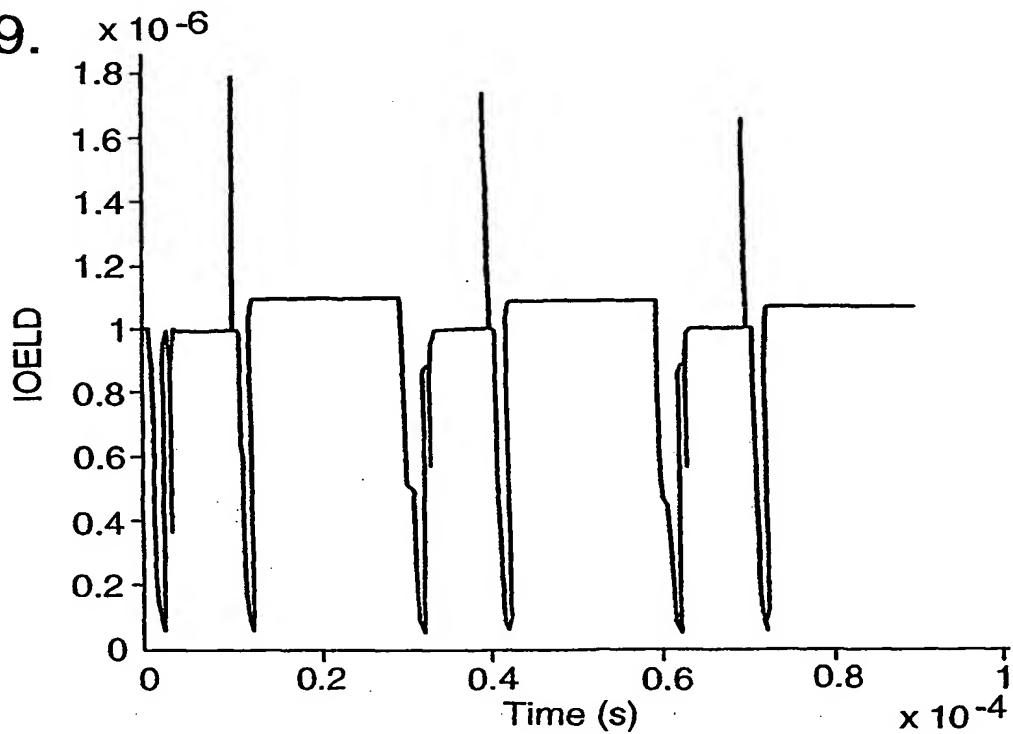
**Fig.8.** SPICE Simulation Result ( $V_{DD} = 12.5V$ ,  $I_{DAT} = 1\mu A$ )**Fig.9.**

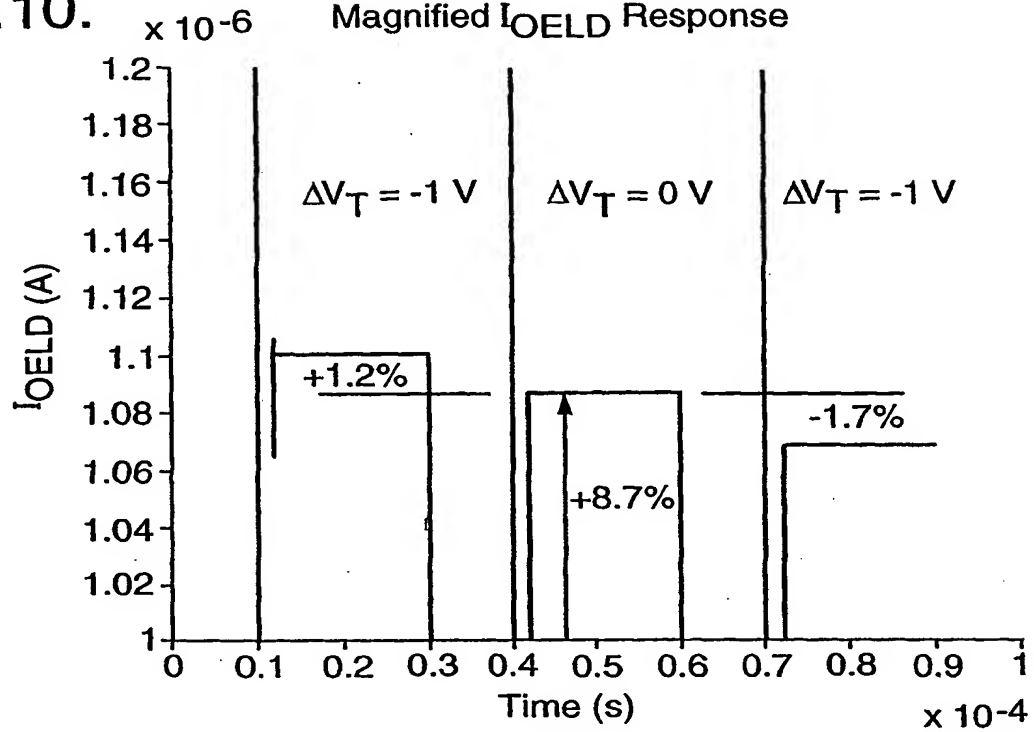
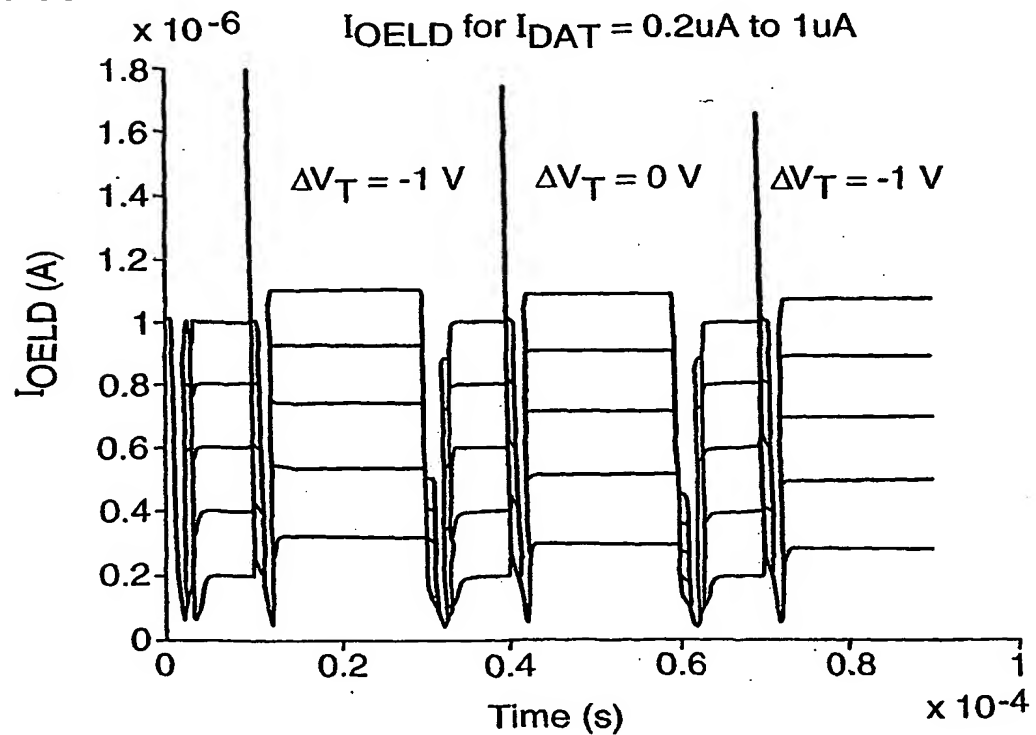
Fig.10. Magnified  $I_{OELD}$  Response

Fig.11.





# INTERNATIONAL SEARCH REPORT

International Application No.

.../GB 01/01460

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 60963/32

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 6096

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	EP 0 923 067 A (SEIKO EPSON CORP) 16 June 1999 (1999-06-16) abstract; figures 11,12  column 36, line 41 -column 37, line 58	1-3, 12-14 4,10,11, 15
X	WO 99 52095 A (FED CORP ;MALAVIYA SHASHI (US)) 14 October 1999 (1999-10-14) abstract; figures 6,7 page 12, line 7 -page 14, line 6	1,12
A	WO 98 48403 A (SARNOFF CORP) 29 October 1998 (1998-10-29) abstract; figure 2	1-3,5, 15,16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

**\* Special categories of cited documents :**

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
- \*E\* earlier document but published on or after the international filing date
- \*L\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

- \*T\* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- \*X\* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- \*Y\* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- \*S\* document member of the same patent family

Date of the actual completion of the international search

9 July 2001

Date of mailing of the international search report

17/07/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Van Roost, L

# INTERNATIONAL SEARCH REPORT

National Application No

JP/GB 01/01460

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 0923067	A	16-06-1999	WO	9840871 A	17-09-1998
WO 9952095	A	14-10-1999	EP	1072032 A	31-01-2001
WO 9848403	A	29-10-1998	US	6229506 B	08-05-2001
			EP	0978114 A	09-02-2000